



Op-Amp Basics

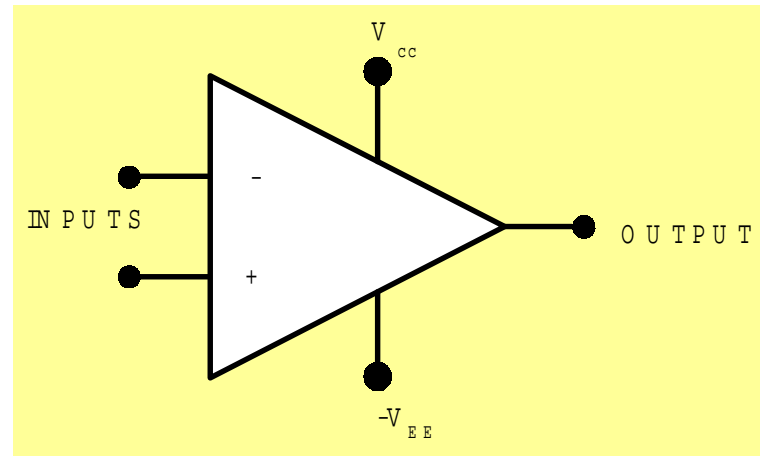
Peggy Alavi
Application Engineer

September 3, 2003



Op-Amp Basics – Part 1

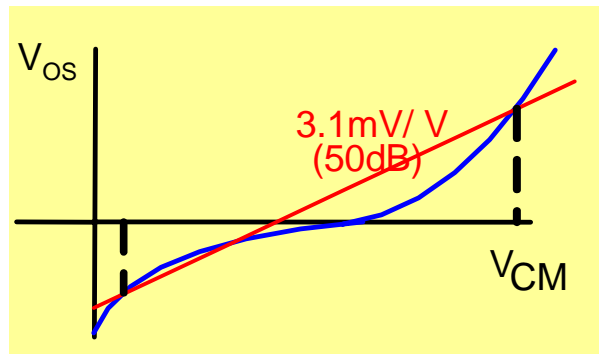
- **Op-Amp Basics**
 - Why op-amps
 - Op-amp block diagram
 - Input modes of Op-Amps
 - Loop Configurations
 - Negative Feedback
 - Gain Bandwidth Product
- **Op-Amp Parameters**
- **Op-Amp Internal Circuit**





Op-Amp Basics – Part 2

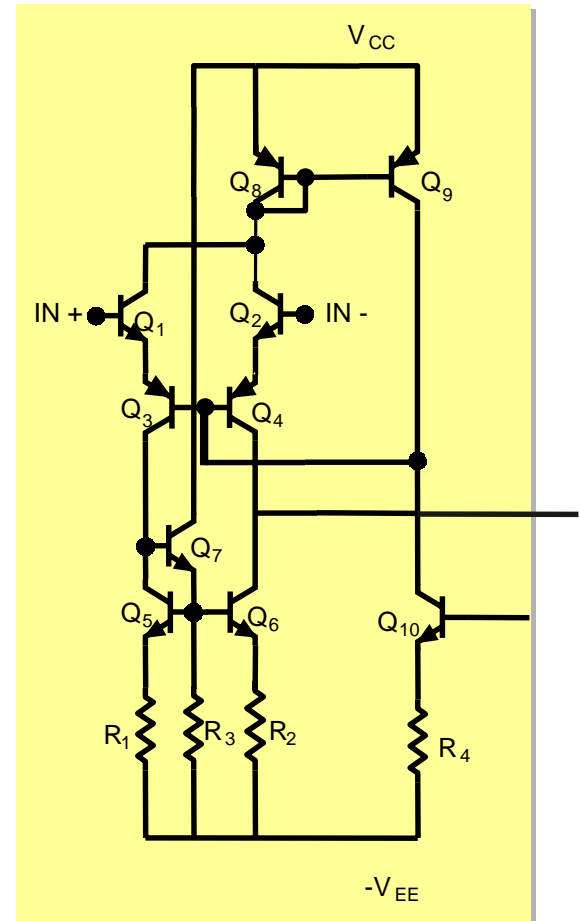
- Op-Amp Basics
- Op-Amp Parameters
 - Input Offset Voltage
 - Input Bias Current
 - Input Offset Current
 - Output Impedance
 - Slew Rate
 - Noise
 - Common Mode Rejection
 - CMRR
 - CMVR
 - PSRR
 - Gain and Phase Margin
 - Abs Max Rating
 - Operating Ratings
- Op-Amp Internal Circuit





Op-Amp Basics – Part 3

- Op-Amp Basics
- Op-Amp Parameters
- **Op-Amp Internal Circuit**
 - Biasing circuit
 - Differential Input Stage
 - Voltage Gain Stage
 - Output Stage





What is an Op-Amp?

- **Inexpensive, efficient, versatile, and readily available building blocks for many applications**
- **Amplifier which has**
 - **Very large open loop gain**
 - **Differential input stage**
 - **Uses feedback to control the relationship between the input and output**



What does an Op-Amp do?

- **Performs many different “operations”**
 - **Addition/Subtraction**
 - **Integration/Differentiation**
 - **Buffering**
 - **Amplification**
 - **DC and AC signals**

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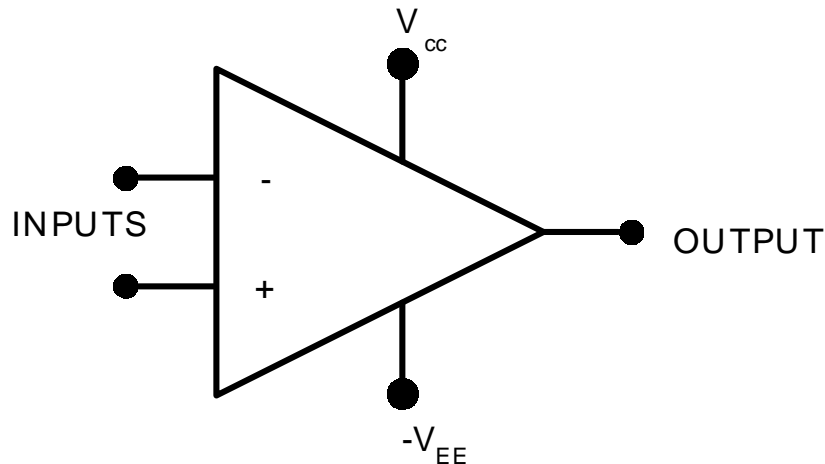
Where is an Op-Amp used?

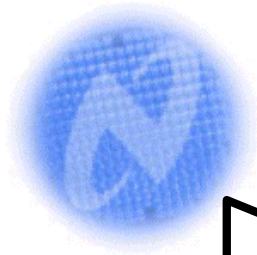
- **Many applications including**
 - **Comparators**
 - **Oscillators**
 - **Filters**
 - **Sensors**
 - **Sample and Hold**
 - **Instrumentation Amplifier**



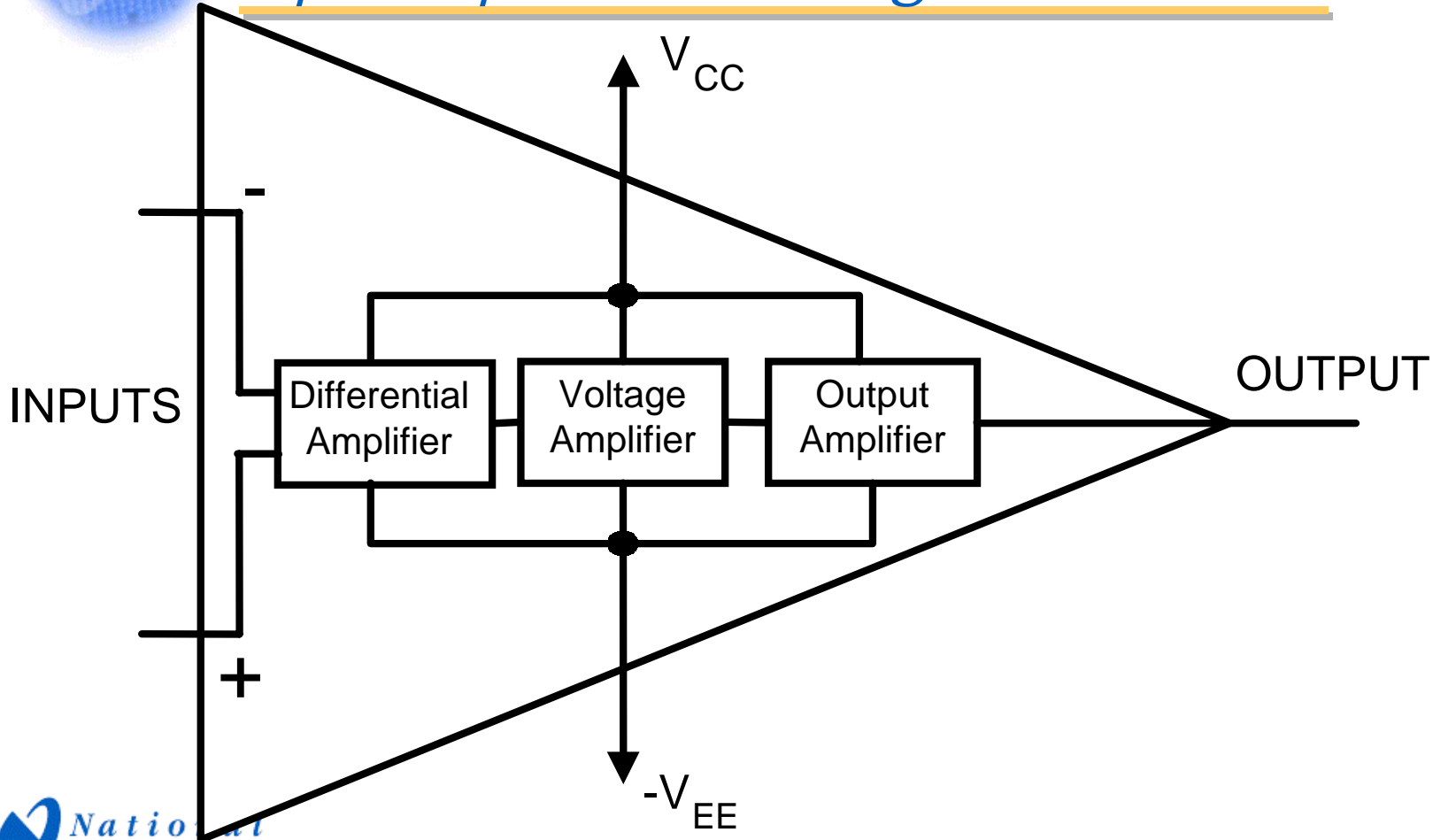
Operational Amplifier

- **Op-Amps must have:**
 - **Very high input impedance**
 - **Very high open loop gain**
 - **Very low output impedance**





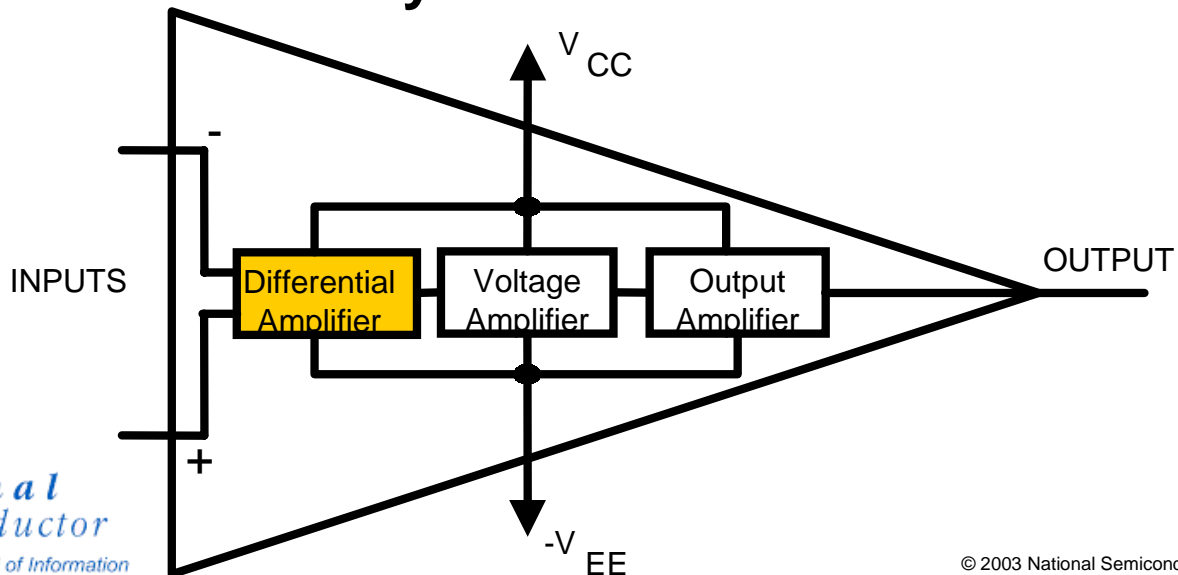
Op-Amp Block Diagram





Differential Amplifier Stage

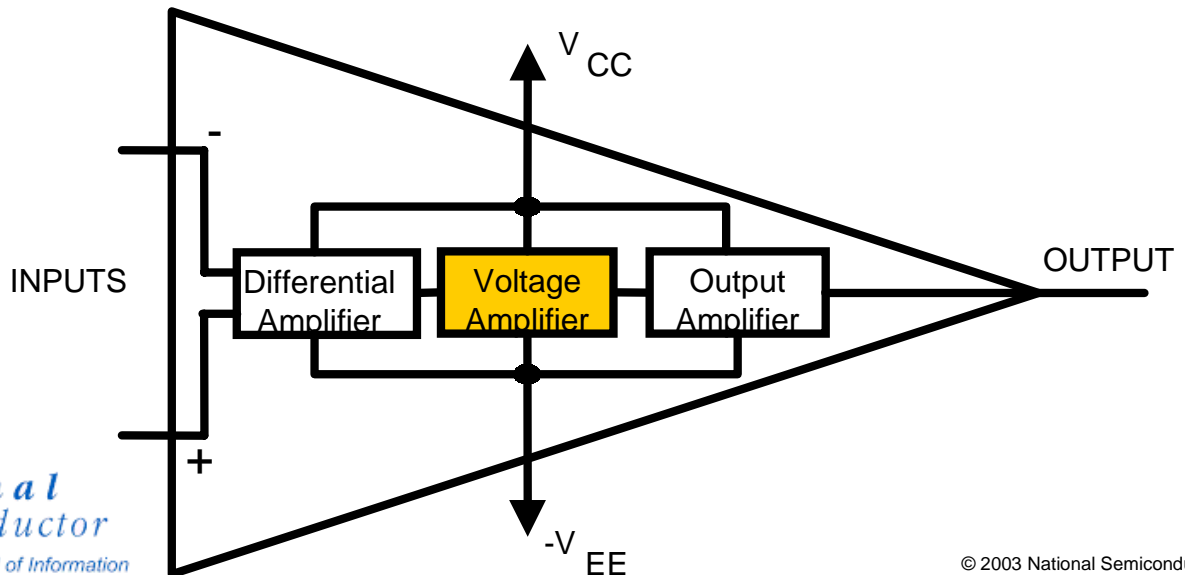
- Provides differential input for the op-amp
- Provides dc gain
- Has very high input impedance
 - Draws negligible input current
 - Enables user to utilize ideal Op-Amp equations for circuit analysis





High Gain Voltage Amplifier

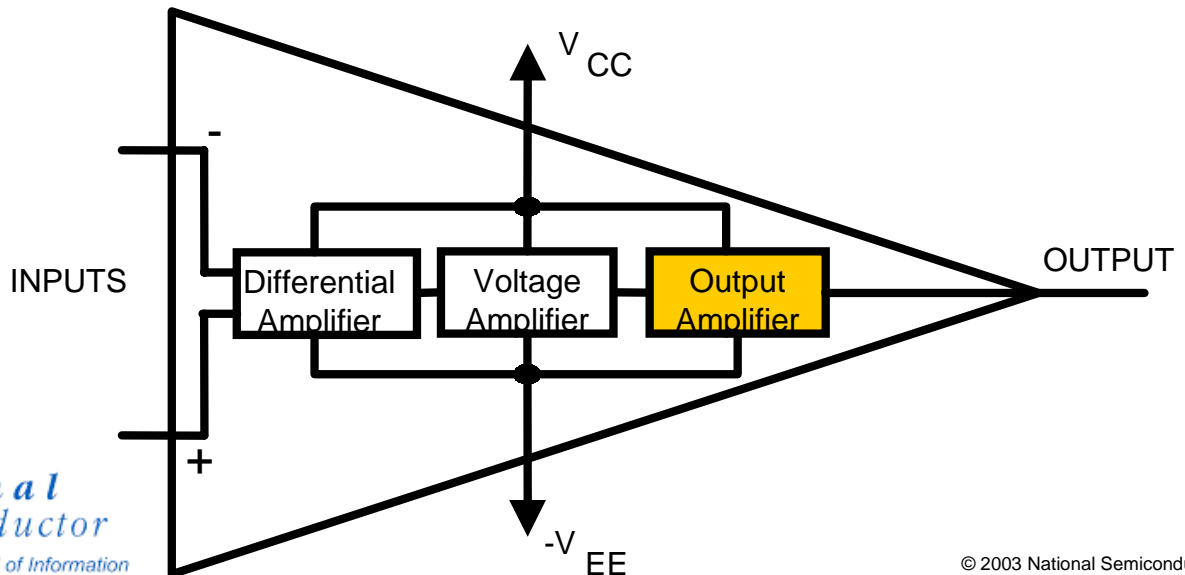
- Provides the “gain” of the amplifier
- Gains up the differential signal from input and conveys it to the output stage





Low Impedance Output Stage

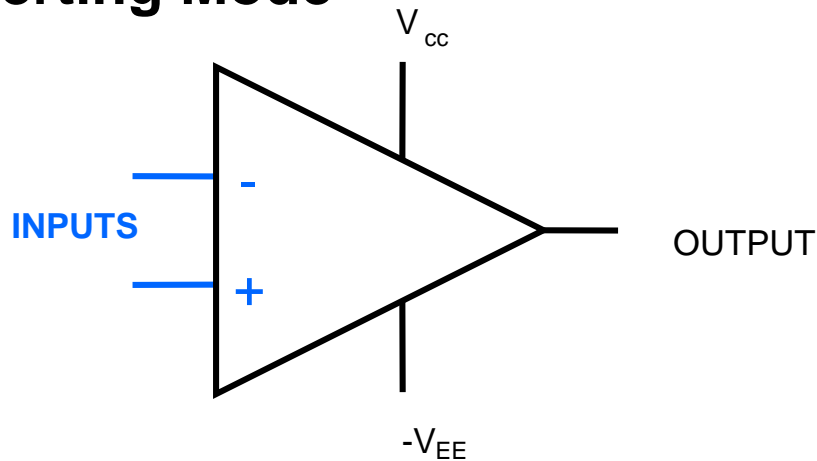
- Delivers current to the load
- Very low impedance output stage
 - To minimize loading the output of the op-amp
- May have short circuit protection





Inputs of Op-Amp

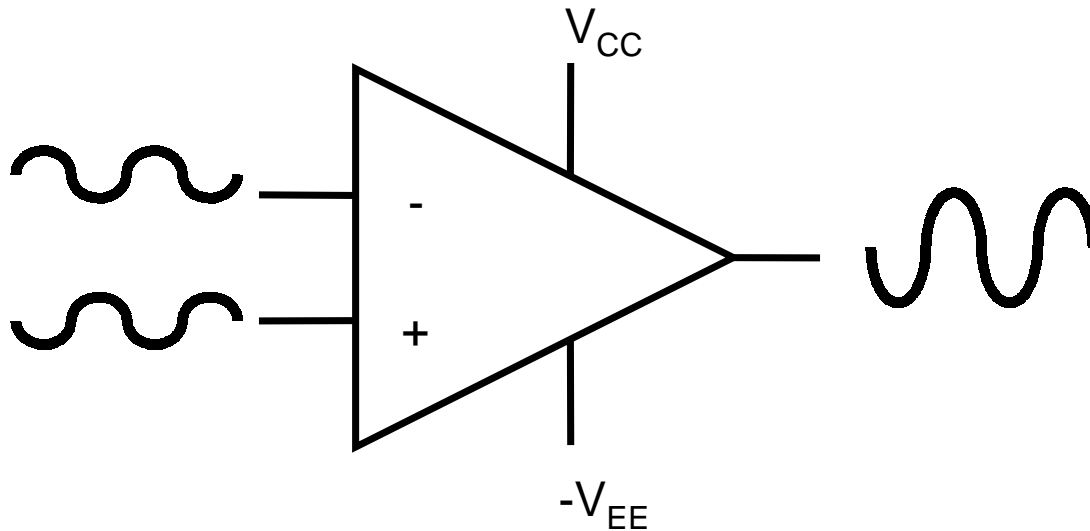
- **Two Input terminals**
 - **Positive Input (Non-Inverting)**
 - **Negative Input (Inverting)**
- **Can be used in three different “input” modes**
 - **Differential Input Mode**
 - **Inverting Mode**
 - **Non-Inverting Mode**





Differential Input Mode

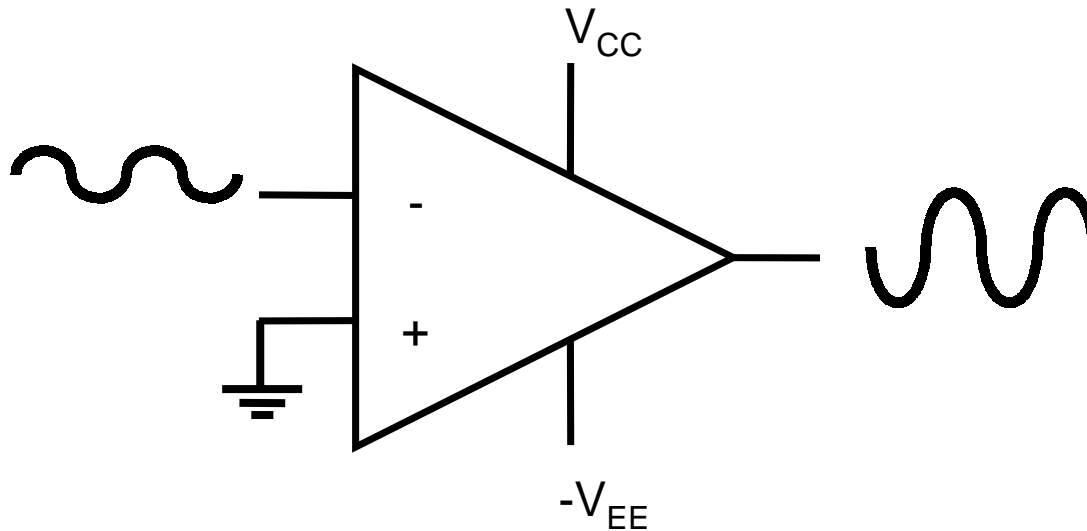
- **Both input terminals are used**
- **Input signals are 180° out of phase**
- **Output is in phase with non-inverting input**





Inverting Mode

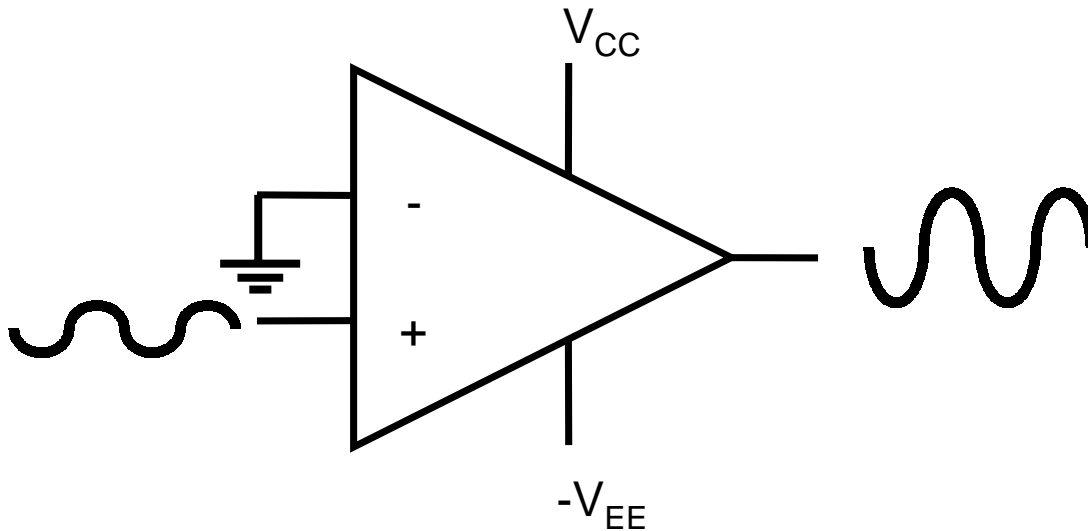
- **Non-Inverting input is grounded (Connected to mid-supply)**
- **Signal is applied to the inverting input**
- **Output is 180° out of phase with input**





Non-Inverting Mode

- Inverting Input is grounded
- Signal is applied to the non-inverting input
- Output is in phase with the input





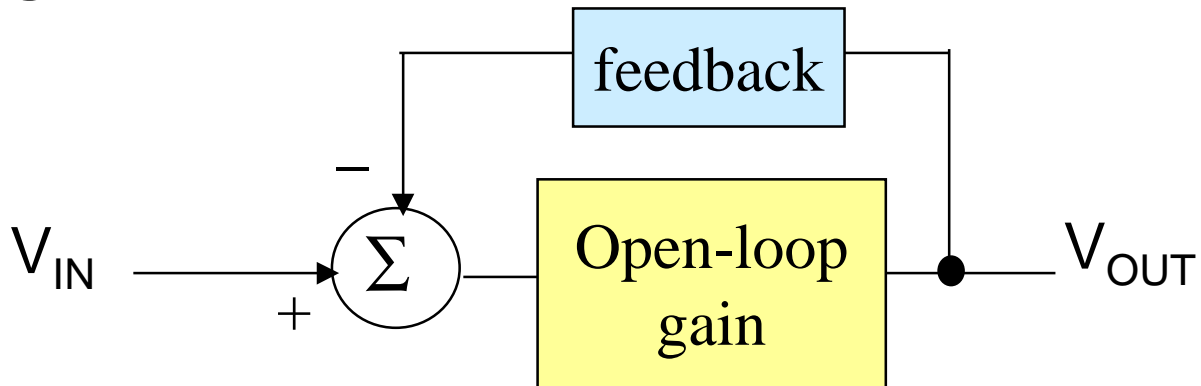
Open Loop VS Closed Loop

- **Open Loop**
 - Very high gain
 - Noise and other “unwanted” signals are amplified by the same gain factor
 - Creates poor stability
 - Used in comparators and oscillators
- **Closed Loop**
 - Reduces the gain of an amplifier
 - Adds stability to the amplifier
 - Most amplifiers are used in this configuration
- **Op-Amps are normally not used in open loop mode**



Closed Loop

- Output is applied “back” into the inverting input
- Op-Amps use negative feedback
 - The “fed back” signal always opposes the effects of the input signal
 - Both inputs will be kept at the same voltage
- Is used in both inverting and non-inverting configurations





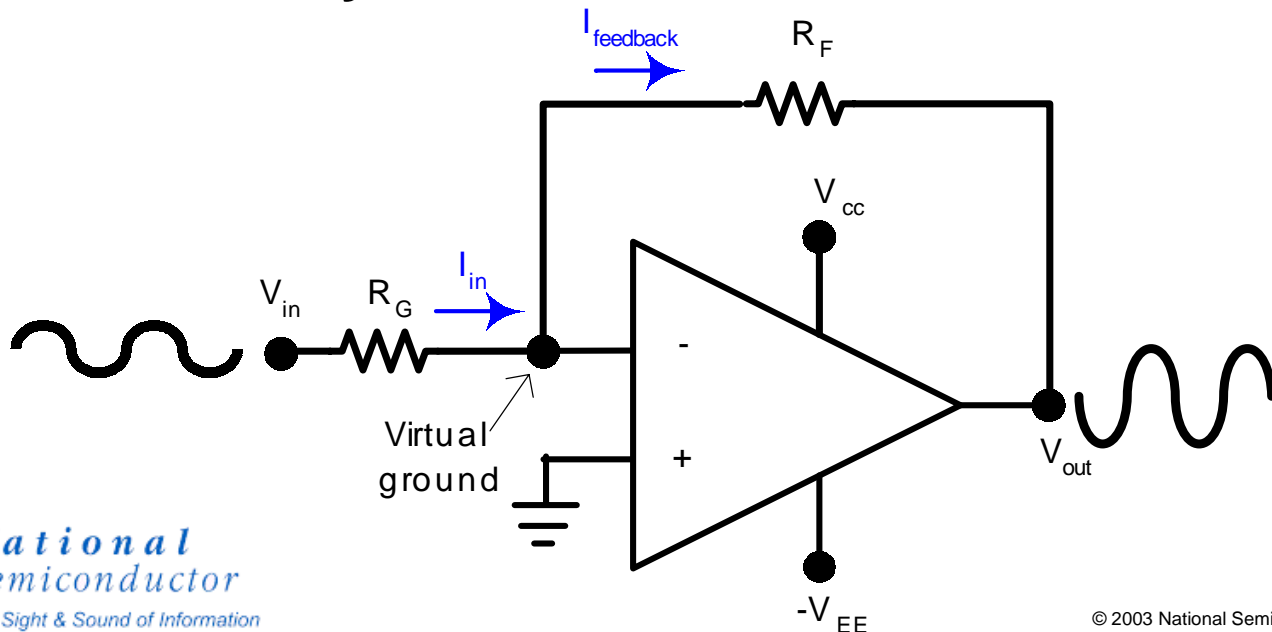
Why Negative Feedback

- **It helps overcome distortion and non-linearity**
- **The relationship between input and output signal is dependent on and controlled by external feedback network**
- **Allows user to “tailor” frequency response to the desired values**
- **It makes circuit properties predictable and less dependent on elements such as temperature or internal properties of the device**



Inverting Closed Loop

- R_F is used to feedback “part” of the output to the inverting input
- Negative input is at virtual ground
- Characteristics of this circuit almost entirely determined by values of R_F and R_G





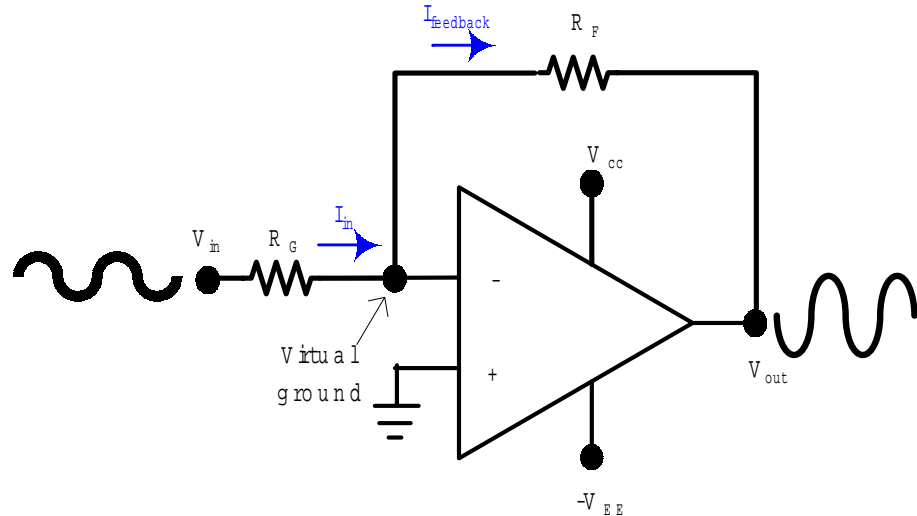
Inverting Closed Loop

$$I_{IN} = \frac{V_{IN}}{R_G}$$

$$I_{feedback} = \frac{-V_{out}}{R_F}$$

$$I_{feedback} = I_{in}$$

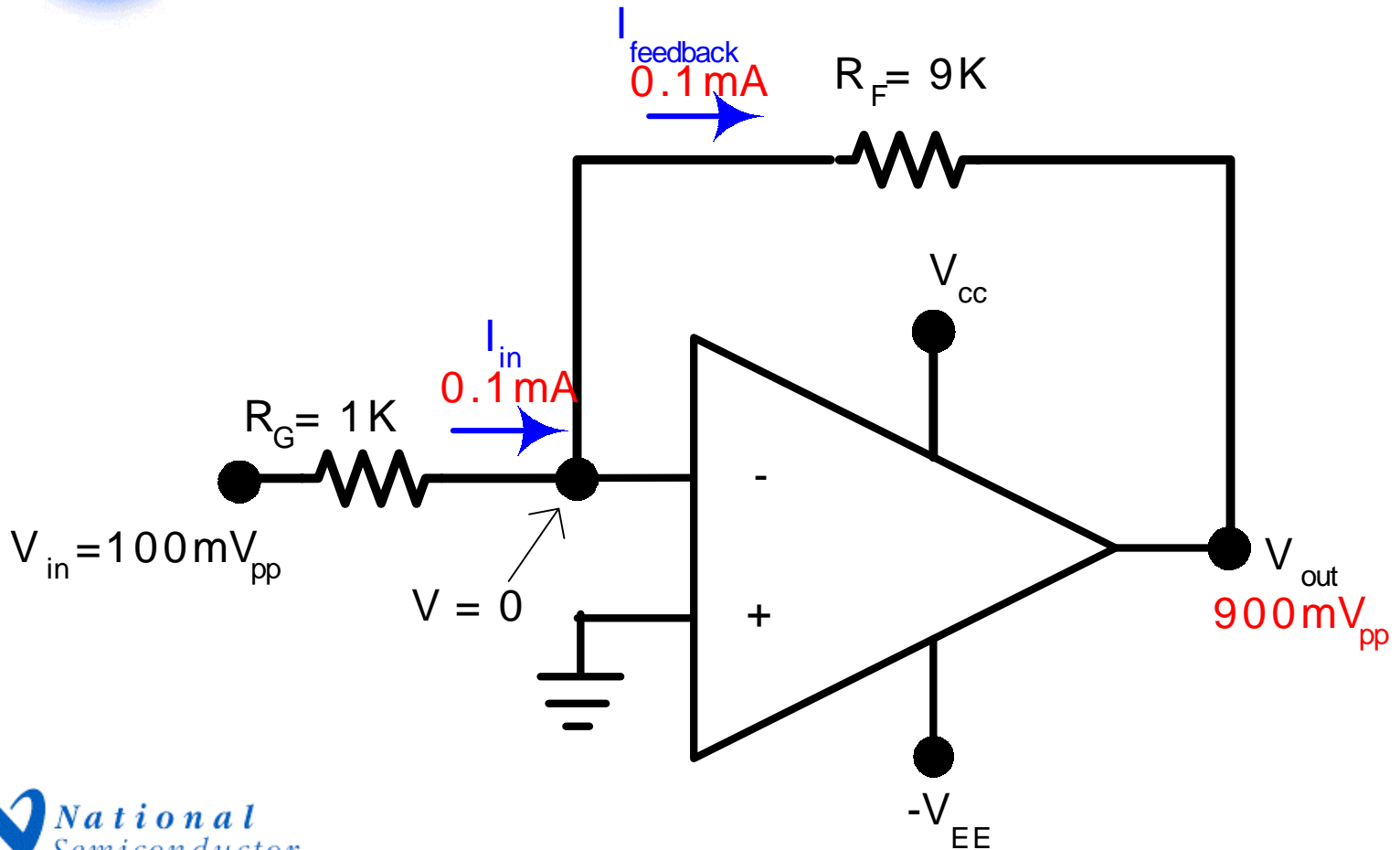
- The two currents must be equal since input bias current is zero



$$\frac{V_{OUT}}{V_{IN}} = \frac{-R_F}{R_G}$$



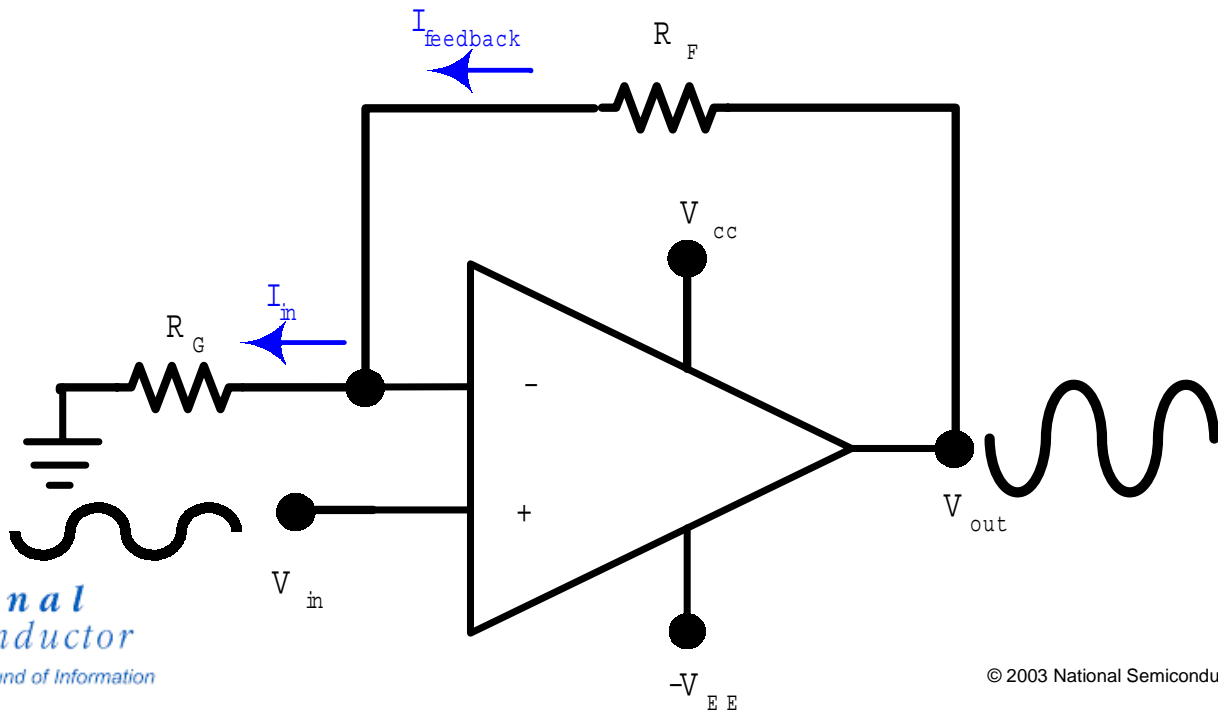
Example: Inverting Amplifier





Non-Inverting Closed Loop

- R_F is used to feedback “part” of the output to the inverting input
- Input, output, and feedback signal in phase
- The feedback *is negative*





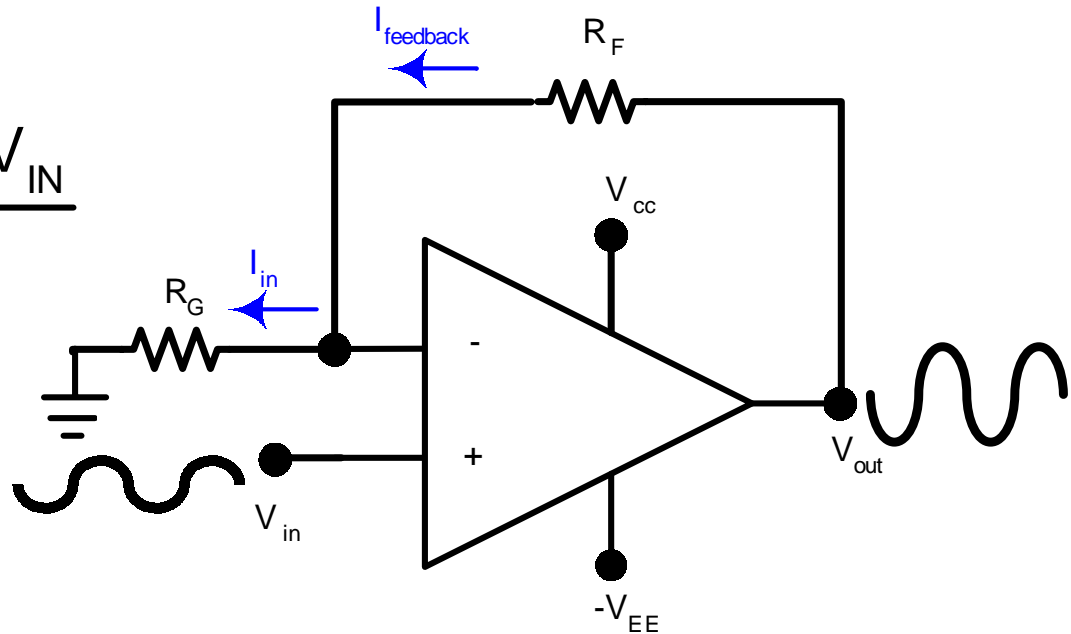
Non-Inverting Closed Loop

$$I_{\text{feedback}} = I_{\text{in}}$$

$$I_{\text{feedback}} = \frac{V_{\text{OUT}} - V_{\text{IN}}}{R_F}$$

$$\frac{V_{\text{IN}}}{R_G} = \frac{V_{\text{OUT}} - V_{\text{IN}}}{R_F}$$

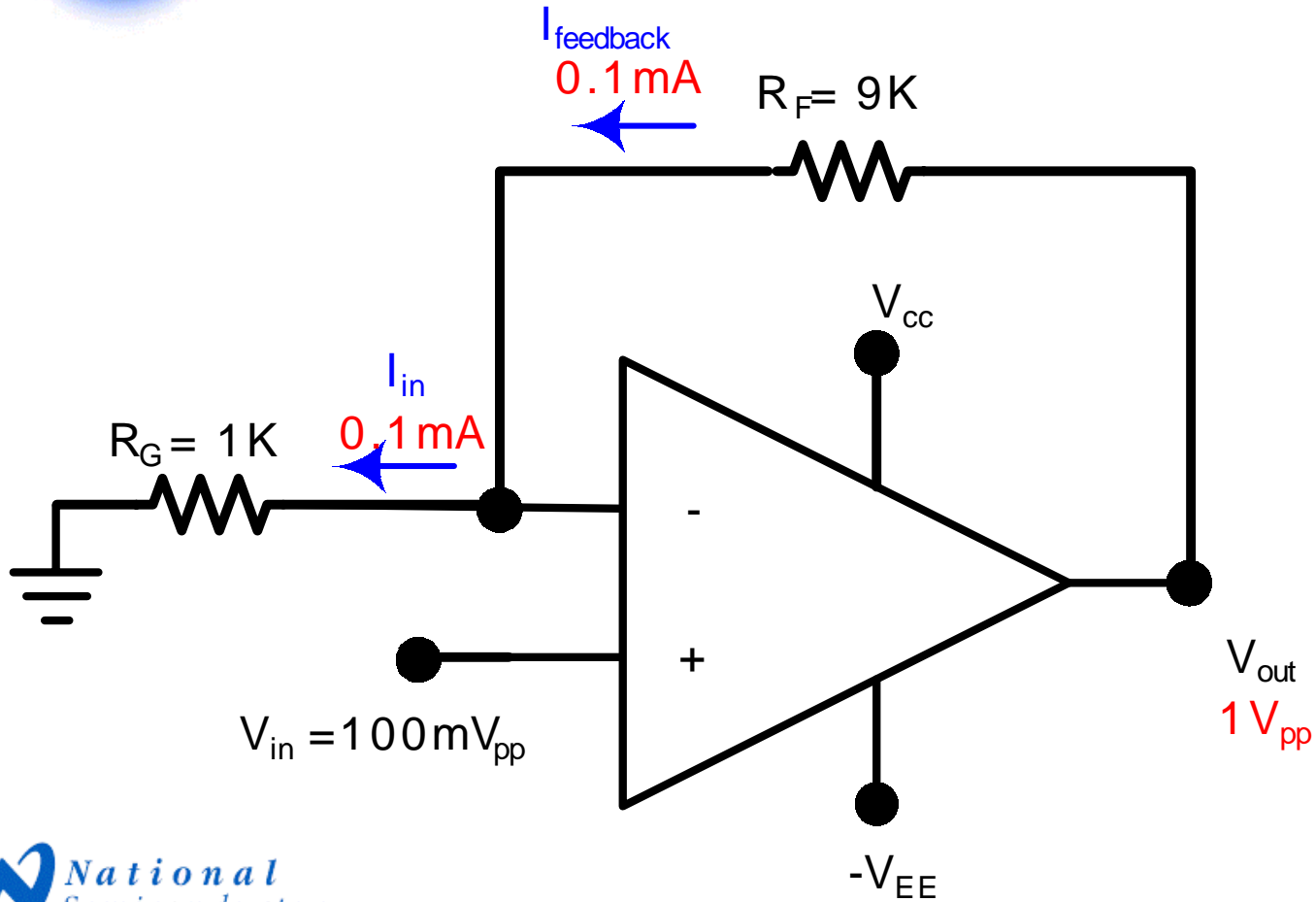
$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = 1 + \frac{R_F}{R_G}$$



- R_F and R_G form a voltage divider



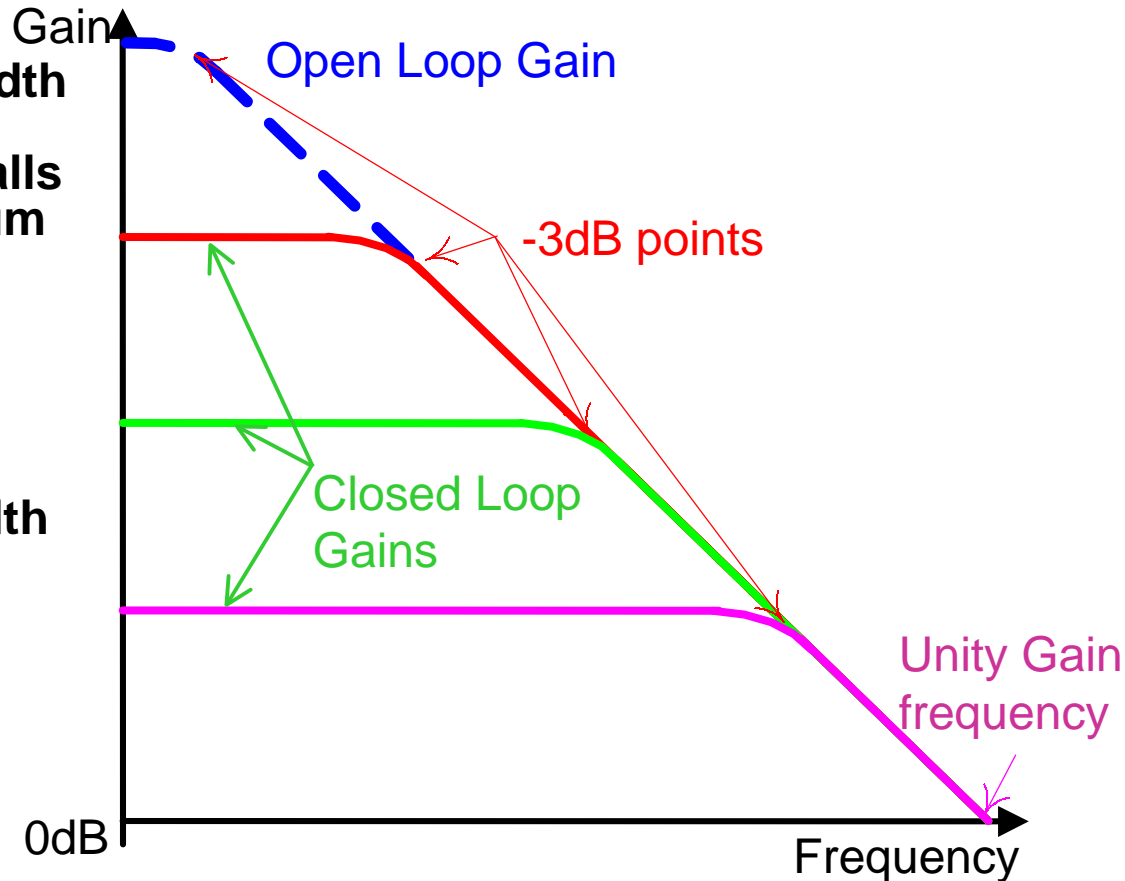
Example: Non-Inverting Amp





Bandwidth Limitation

- Frequency bandwidth is measured at the point where gain falls to 0.707 of maximum signal
 - The -3dB bandwidth
- Open loop configurations are *extremely* bandwidth limited
- Closed loop configuration significantly increases an op-amp's bandwidth





Gain Bandwidth Product

- **Gain X Bandwidth = Unity Gain Frequency**
- **Known as GBWP**
- **Used to determine an op-amp's bandwidth in an application**
 - **GBWP is specified in datasheet**
 - **Gain is set by user**



Op-Amp Parameters



Input Offset Voltage

- Ideally, output at mid-supply when the two inputs are equal
- Realistically, a voltage will appear on output when both input voltages are the same
- Minimal voltage difference “offset” on inputs will set the output to mid-supply again
- This is Input Offset Voltage

V_{OS}



Input Bias Current

- **Ideally should be zero**
- **Positive input bias current:**
 - Small current seen on the non-inverting input of an amplifier
- **Negative input bias:**
 - Small current seen on the inverting input of an amplifier
- **Input Bias Current:**
 - Average of currents on inputs of an amplifier

IBIAS



Input Offset Current

- **Ideally input currents should be equal to obtain zero output voltage**
- **Realistically, to set output to zero, one input would require more current than the other**
- **Input offset current: Difference between the two input currents to achieve zero output**

I_{os}



Output Impedance

- **Ideally should be zero**
- **It is usually “assumed” to be zero**
 - **This way op-amp behaves as a voltage source**
 - **Op-amp capable of driving a wide range of loads**

Z_{OUT}

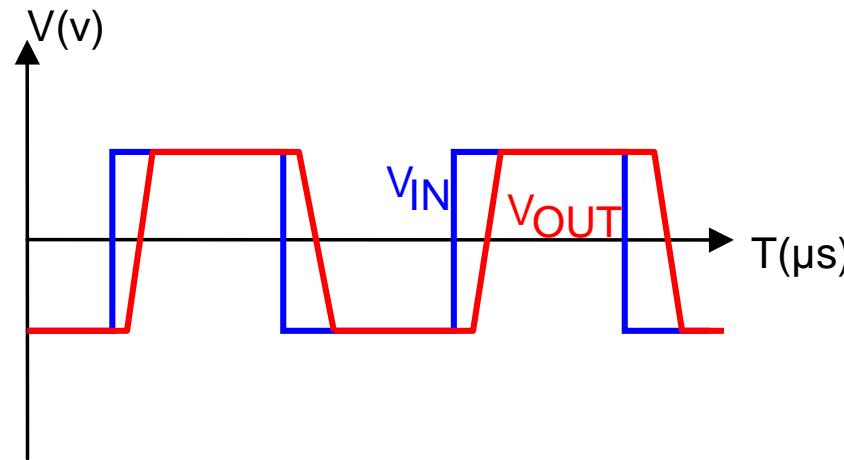


Slew Rate

- **Maximum rate of change of the output voltage per unit time**

- $$SR = \frac{V_{OUT}}{t}$$

- **Expressed in**
$$\frac{V}{\mu S}$$



- **Basically says how fast the output can “follow” the input signal**



Internal Noise

- **Caused by internal components, bias current, and drift**
- **Noise or “unwanted” signal is amplified along with the “wanted” signal**
 - **Noise gain = $1 + \frac{R_F}{R_G}$**
- **Can be minimized by keeping feedback and input series resistor values as low as possible**
 - **Bypass capacitor on feedback resistor reduces noise at high frequencies**



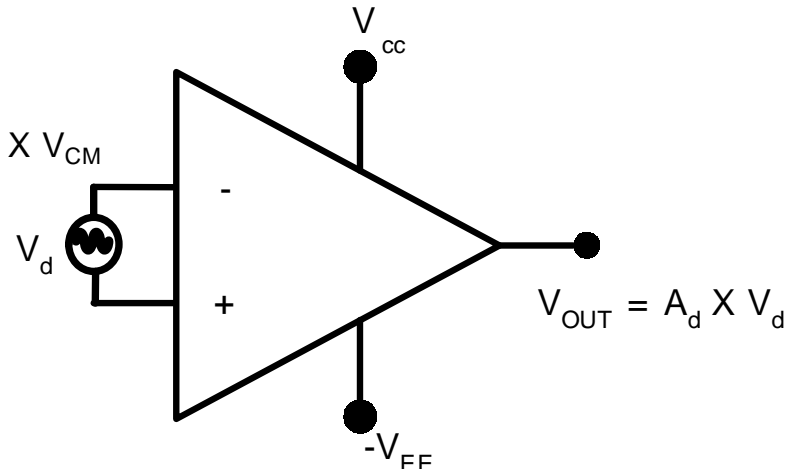
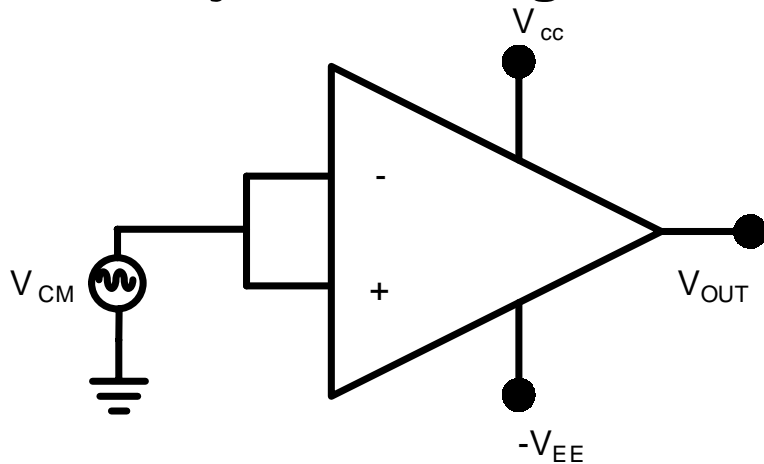
External Noise

- **Caused by electrical devices and components**
 - **Power Supply Noise**
 - **Resistor Noise**
- **Proper circuit construction technique will minimize this noise**
 - **Adequate shielding**
 - **Reduce Resistor values when possible**
 - **Use 1% or higher accuracy resistors**



Common Mode Rejection

- Feature of differential amplifiers
- Common Mode signal is when both inputs have the same voltage “common voltage”
- Output should be zero in this case, op-amp should “reject” this signal





Common Mode Rejection Ratio

- **CMRR**
- **Ratio of differential gain to common mode gain when there is no differential voltage on the input**
- **Usually expressed in dB**
- **Decreases with frequency**
 - **Common mode gain increases with frequency**



Common Mode Rejection Ratio

- **Ability of an op-amp to reject common mode signal while amplifying the differential signal**

- $$\text{CMRR} = 20 \text{ LOG} \left| \frac{A_d}{A_{\text{CM}}} \right| = 20 \text{ LOG} \left| \frac{\Delta V_{\text{OS}}}{\Delta V_{\text{CM}}} \right|$$

A_d : Differential Gain

A_{CM} : Common Mode Gain

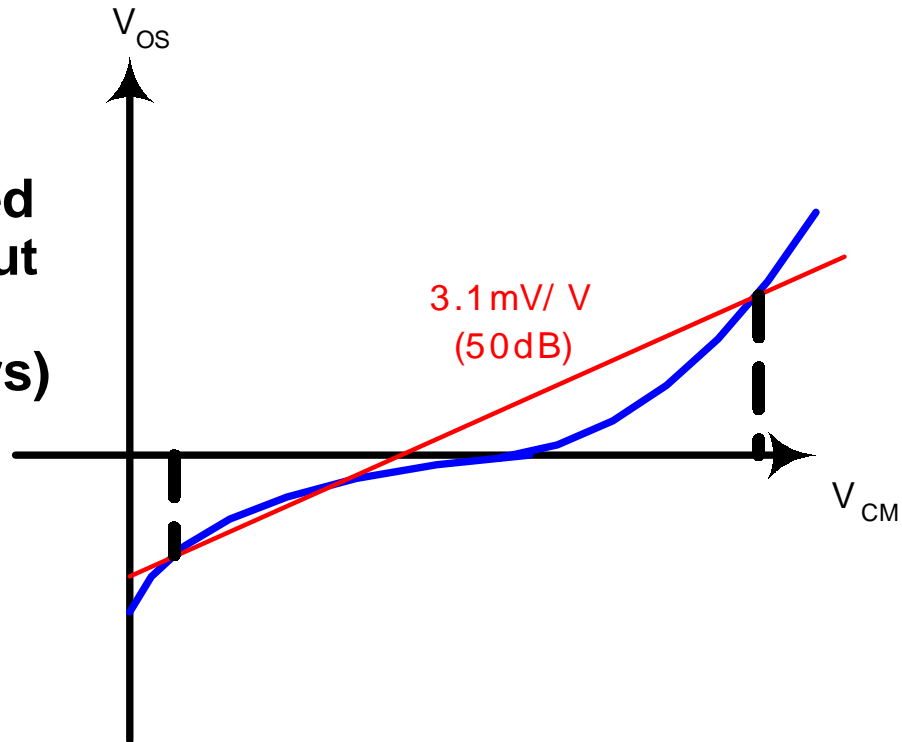
V_{OS} : Offset Voltage

V_{CM} : Common Mode Voltage



Common Mode Voltage Range

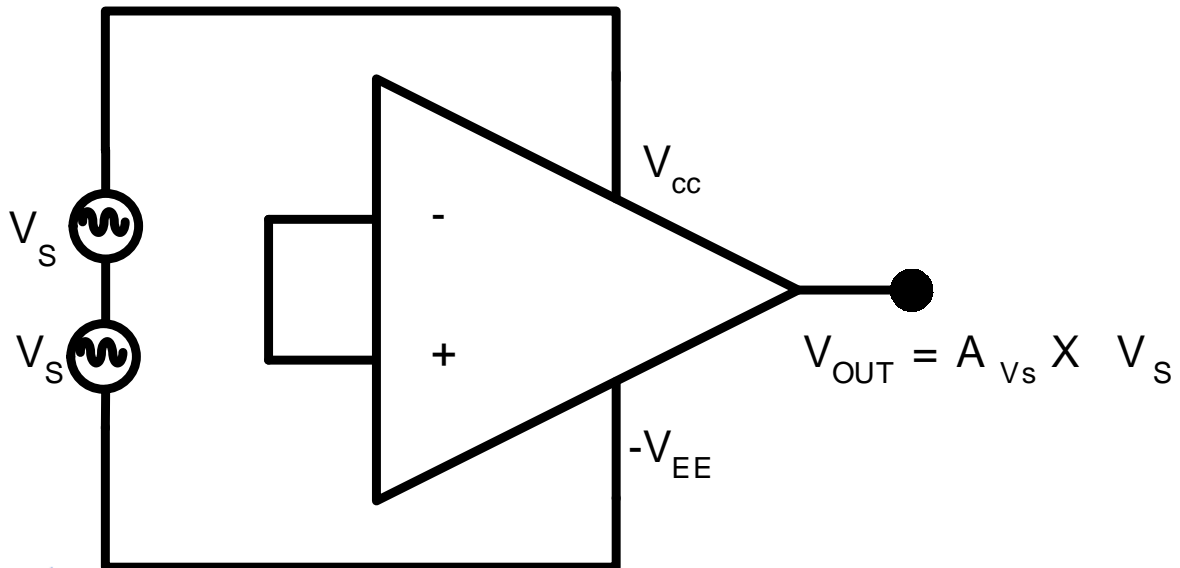
- Range of input voltage, V_{CM} , for which the differential pair behaves as a linear amplifier
 - Upper limit determined by one of the two input transistors saturating (DC value of collectors)
 - Lower limit is determined the by transistor supplying bias current





Power Supply Rejection Ratio

- **Ratio of differential gain to small signal gain of the power supply**
 - **Ratio of change in power supply voltage to the change in offset error**



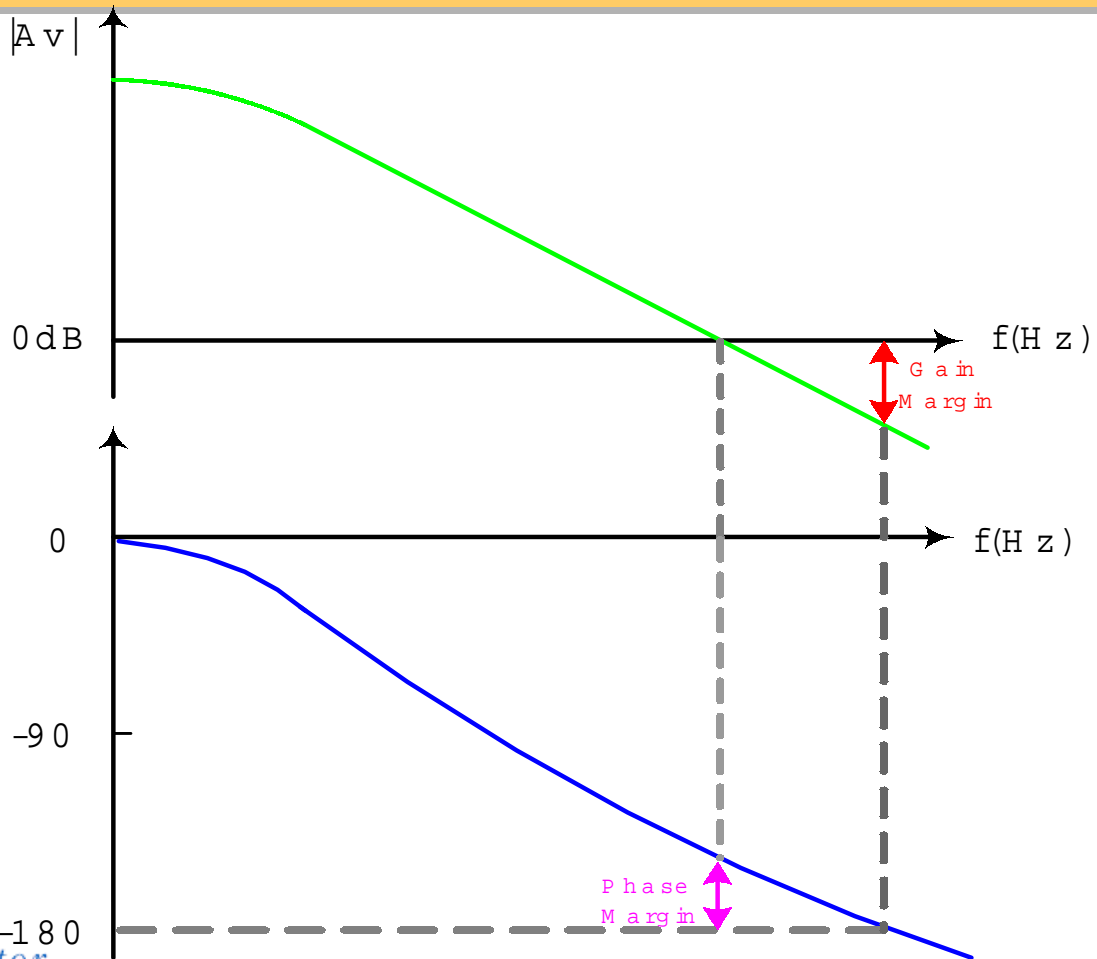


Gain and Phase Margin

- **Gain Margin:**
 - Gain of the amplifier at the point where there is a 180° phase shift
 - If gain more than unity, amplifier unstable
 - In dB this means negative gain stable
- **Phase Margin:**
 - Difference between phase value at unity gain (0dB) and 180°
 - If at 0 dB, phase lag is greater than 180° , amplifier is unstable



Gain and Phase Margin





Absolute Maximum Rating

- **“Maximum”** means the op-amp can safely tolerate the maximum ratings as given in the datasheet without damaging its internal circuitry
- Operation of op-amp beyond the maximum rating limits will permanently damage the device

LMV721/LMV722

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/

THD	Total Harmonic Distortion	$f = 1\text{kHz}, A_v = 1$ $R_L = 600\Omega, V_O = 1\text{V}_{PP}$	0.001	%
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Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF. Machine model, 200 Ω in series with 100 pF.

Note 3: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the



Operating Ratings

- **Conditions under which an amplifier is functional; however specific performance guarantees do not apply to these conditions**
 - i.e. Table guarantee $\pm 2.5V$
Operating Rating $V_s = \pm 5V$

Operating Ratings (Note 3)

Supply Voltage	2.2V to 5.0V
Temperature Range	$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$
Thermal Resistance (θ_{JA})	
Silicon Dust SC70-5 Pkg	440 $^{\circ}\text{C/W}$

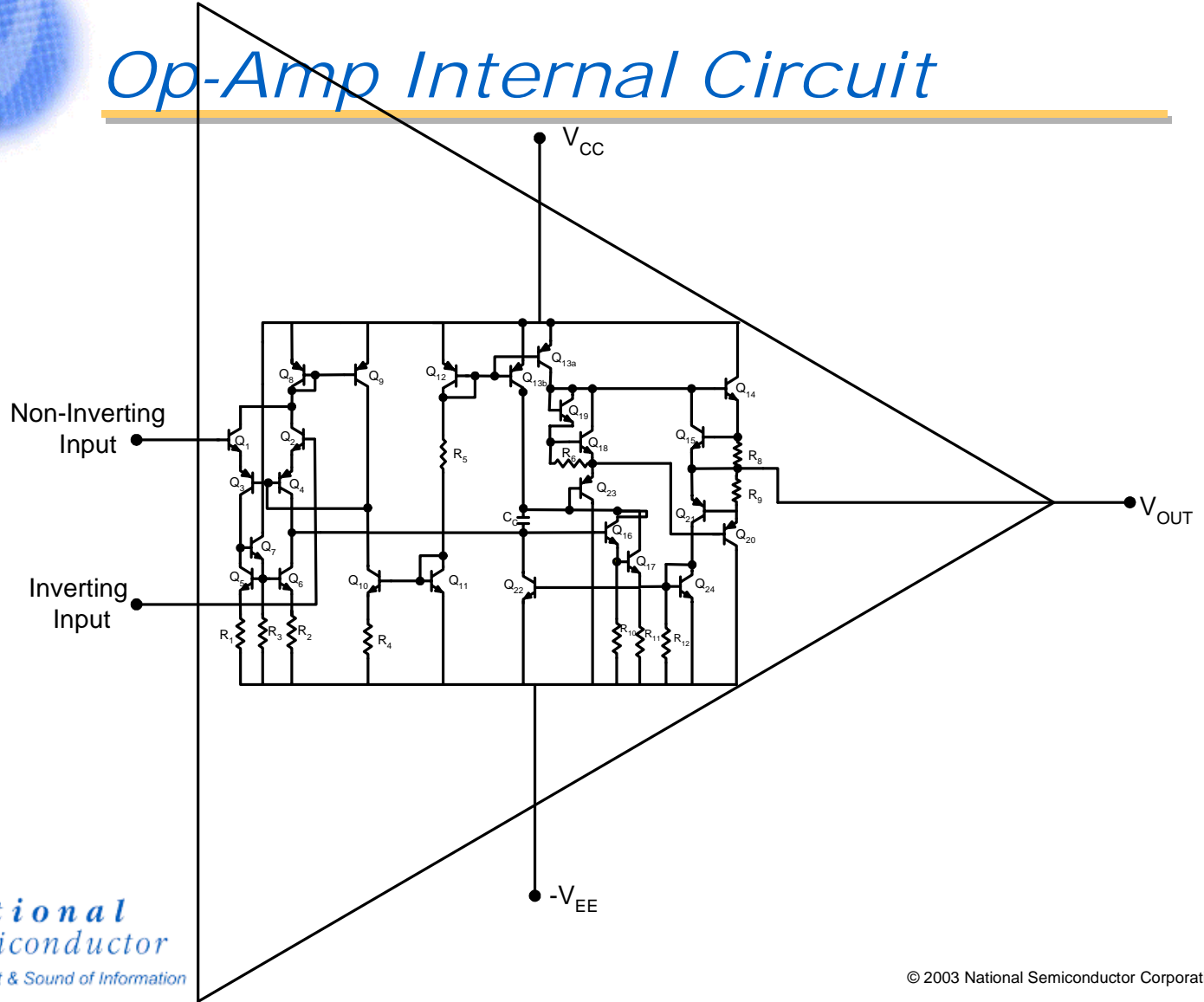
Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 $^{\circ}\text{C}$. Output currents in excess of 30 mA over long term may adversely affect reliability.



Op-Amp Internal Circuit

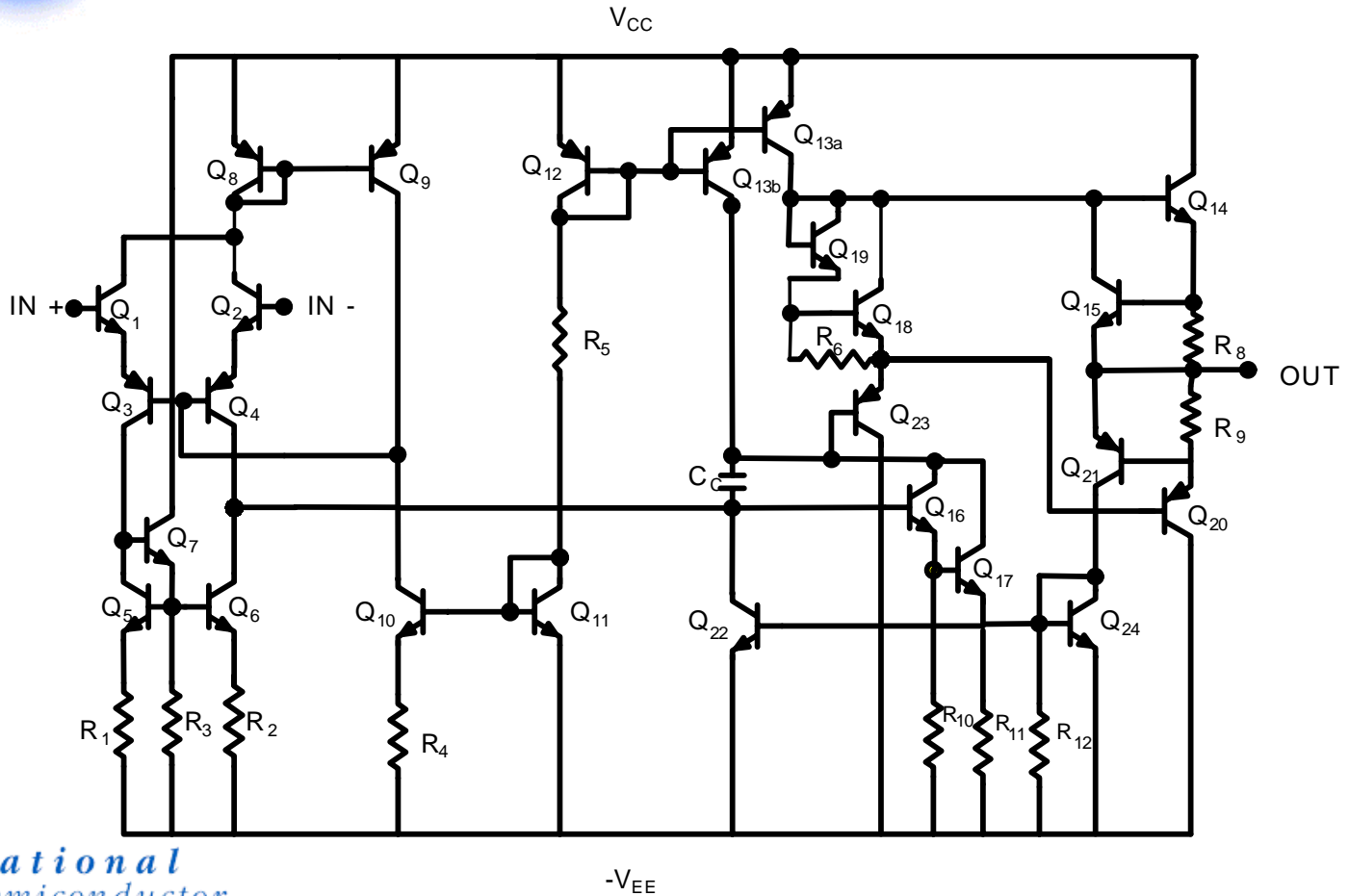


Op-Amp Internal Circuit





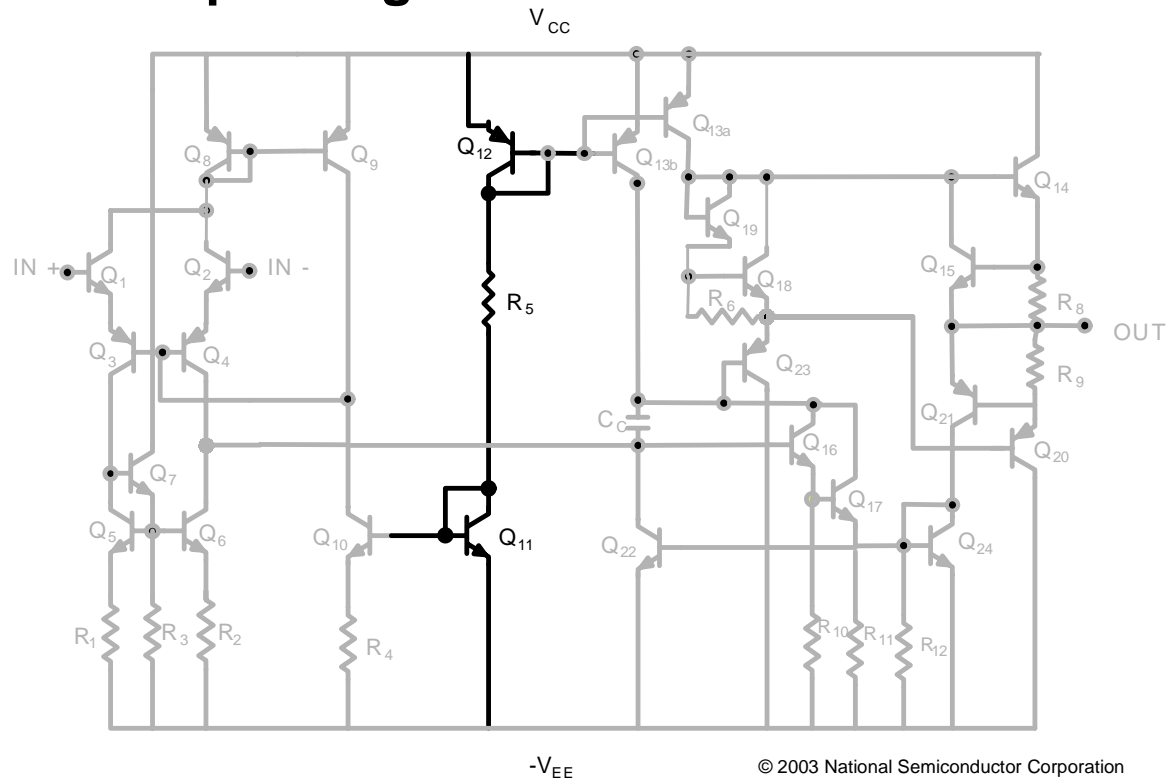
Internal Circuit of Classic Op-Amp LM741





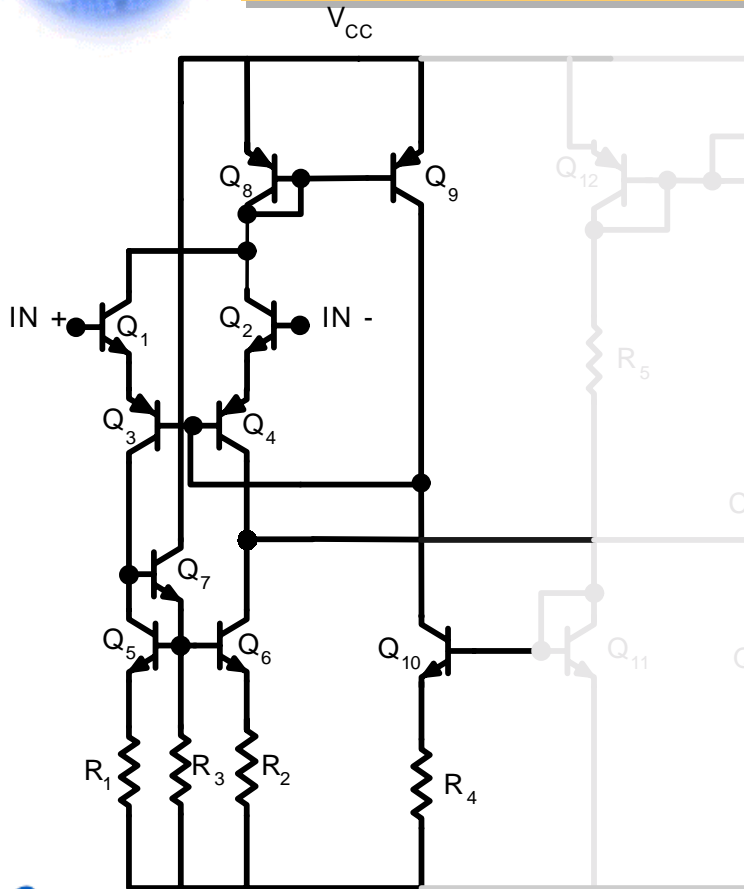
Biasing Circuit

- This branch of provides the current
- Q_{12} , Q_{11} , and R_5
- Current delivered to input stage through Q_{11}





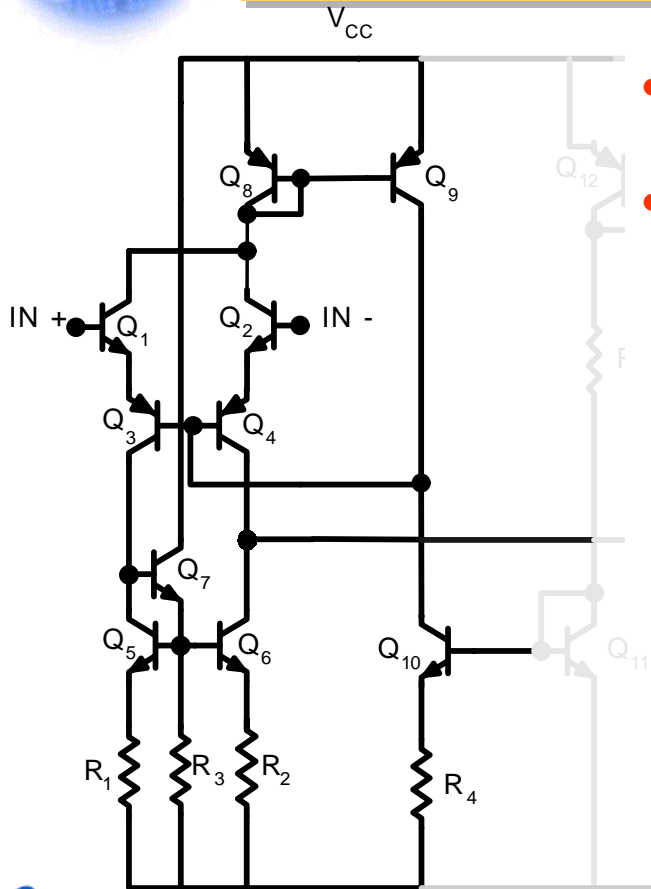
Op-Amp Internal Circuit Differential Input Stage - 1



- Q_{10} mirrors Q_{11} current and delivers it to Q_3 and Q_4 base
- Q_3 and Q_4 in series with Q_1 and Q_2 form the differential input
- Q_1 and Q_2 connected as emitter followers
 - High input impedance
- Q_3 and Q_4 provide dc level shifting
 - Also protect Q_1 and Q_2 form emitter-base junction break down



Op-Amp Internal Circuit Differential Input Stage - 2

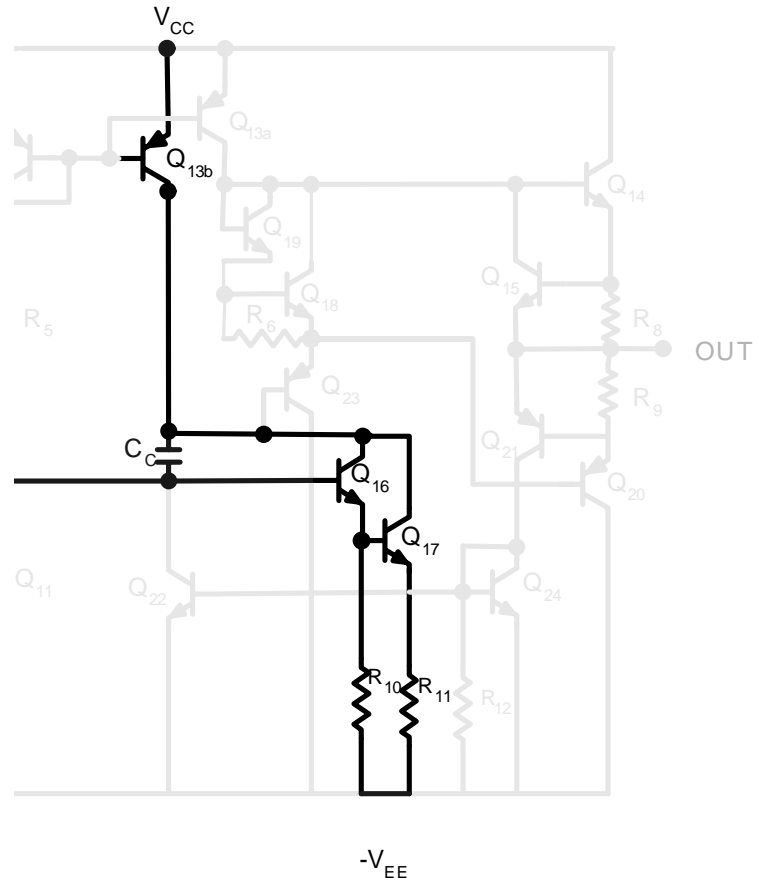


- Q_5 , Q_6 , Q_7 , R_1 , R_2 , and R_3 load circuit of input stage
- High resistance load
 - Converts differential signal to single ended
 - Provides gain
 - Single ended output is taken at Q_6 collector



Op-Amp Internal Circuit Voltage Gain Stage - 1

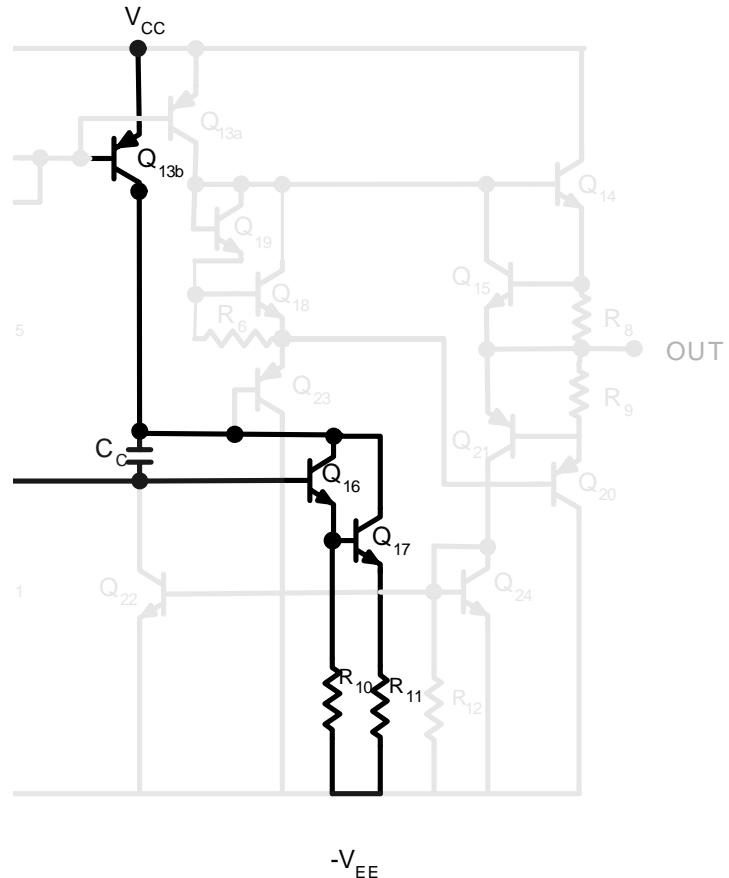
- **Q₁₆ emitter follower**
 - Gives 2nd stage high input resistance
 - Minimizes loading of input stage
 - Prevents gain loss
- **Q₁₇ common emitter amplifier**
 - Load : high output resistance of pnp (Q_{13b}) || with input resistance of Q₂₃
- **Output of 2nd stage at collector of Q₁₇**





Op-Amp Internal Circuit Voltage Gain Stage - 2

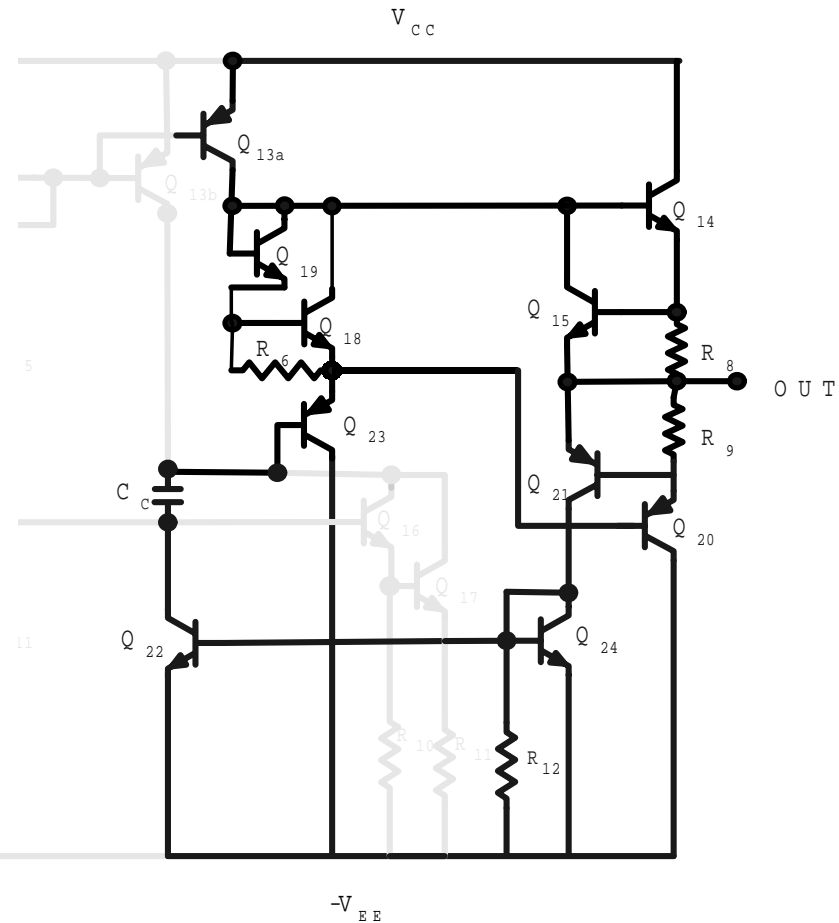
- **Active load: use of transistor current source as a load resistance**
 - high gain without high load resistance
 - Saves chip area
 - No need for high supply voltage
- **C_C Miller compensation capacitor**
 - Frequency compensation





Op-Amp Internal Circuit Output Stage - 1

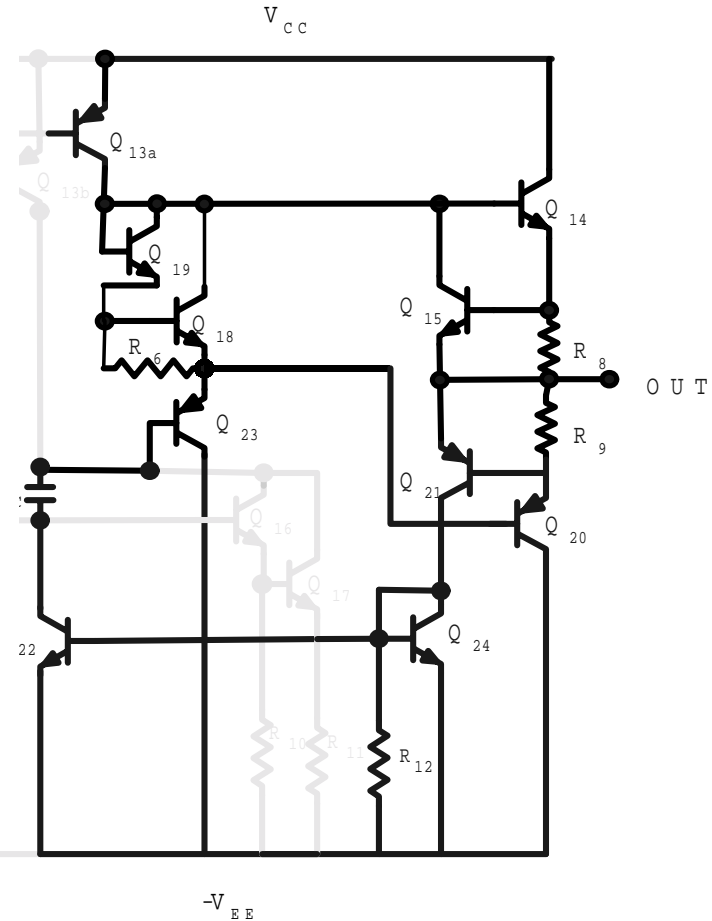
- **Q_{14} (Source transistor) and Q_{20} (Sink transistor) form the output complementary symmetry stage**
 - Output pin between R_8 and R_9
 - Output goes positive, Q_{14} conducts more
 - Pulls output towards positive supply
 - Output goes negative, Q_{20} conduct more
 - Pulls output towards negative supply





Op-Amp Internal Circuit Output Stage - 2

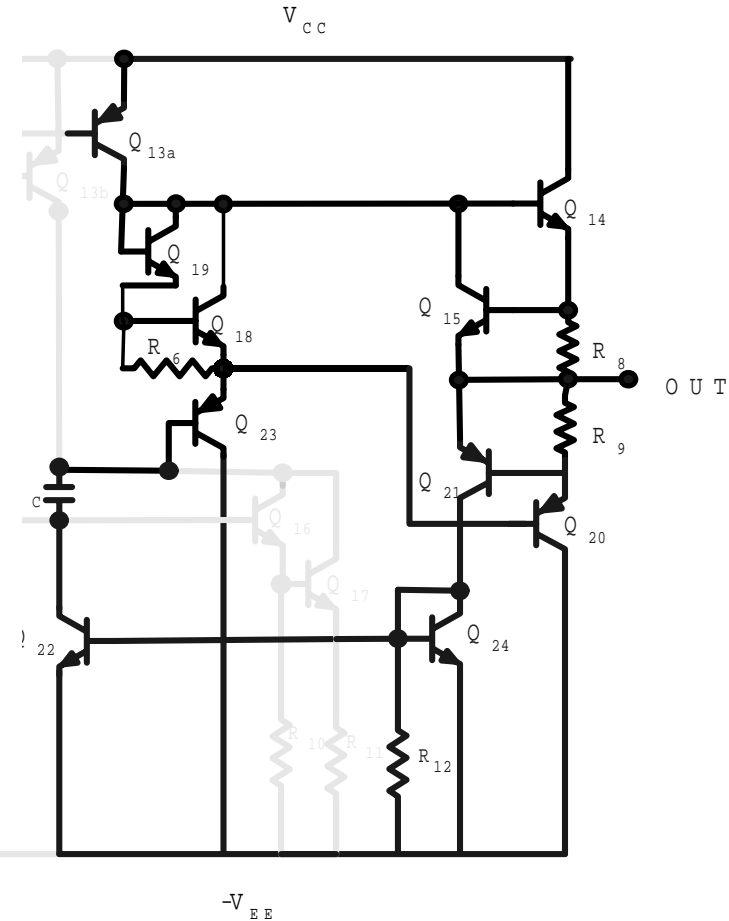
- Q_{15} current limiting protection, short circuit protection, for Q_{14}
- Q_{21} current limiting protection, short circuit protection, for Q_{20}
- Q_{18} and Q_{19} bias the output transistor in linear region
 - Fed by Q_{13a}





Op-Amp Internal Circuit Output Stage - 3

- Q_{23} emitter follower
 - Minimizes loading on output of 2nd stage
- Class AB output stage
- Q_{14} and Q_{20} have larger area
 - Supplies fairly large load currents
 - Minimal power usage
 - Negligible temperature effect
- Low output impedance





Conclusion

During this presentation we covered

- **Basic op-amp configurations**
- **Basic parameters of op-amps**
- **Internal Circuit of the 741**

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